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SECTION III—REMARKS

This amendment is submitted in response to the final Office Action mailed May 5, 2006. Claims 1, 12 and 34 are amended, and claims 1-22 and 34-44 remain pending in the application. Applicants respectfully request reconsideration of the application and allowance of all pending claims in view of the above amendments and the following remarks.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1-2, 8-9, 11-13, 16, 19-20 and 22 as anticipated under 35 U.S.C. § 102(e) by U.S. Patent Application Publication No. 2004/0253809 to Yao *et al.* ("*Yao*"), and anticipated under 35 U.S.C. § 102(b) by U.S. Patent Application Publication No. 2002/0115283 to Ho *et al.* ("*Ho*") and U.S. Patent No. 6,495,44 to Lopatin *et al.* ("*Lopatin*"). Applicants respectfully traverse the Examiner's rejections. A claim is anticipated only if each and every element, as set forth in the claim, is found in a single prior-art reference. MPEP § 2131; *Verdegaal Bros. v. Union Oil of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). As explained below, *Yao*, *Ho* and *Lopatin* cannot anticipate these claims because none discloses every element and limitation recited in the claim.

Claim 1, as amended, recites a process combination including:

> providing a wafer, *the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer*;

exposing the barrier layer;

placing the wafer in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer;

immersing the holder and the wafer in the electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte; and

applying an electrical potential between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed.

(emphasis added). None of the references cited by the Examiner discloses every elem ent and limitation in this claim. *Yao* discloses a process for forming a semiconductor struc ure using a combination of planarizing methods and electropolishing. *Yao*, however, discl ses that its barrier layer is deposited directly on a dielectric layer without any interve ing layers. *Yao* thus cannot disclose a combination including "an inter-layer dielectric (I D) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposite on the under-layer and a conductive layer deposited on the barrier layer." Moreover, *Yao* oes not disclose that the wafer should be put in any kind of holder and discloses that electr yte should be sprayed onto the wafer (*see* Fig. 5). *Yao* therefore cannot disclose, teac or suggest a combination including "placing the wafer in a holder that seals the edges the of, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer." Finally, *Yao* discloses that its seed layer shoul be removed by electropolishing, but says nothing about electropolishing its barrier layer; *Yao*, in fact, discloses that the barrier layer should be removed by etching (*see* paragr phs

[0041], [0042]). *Yao* therefore cannot disclose, teach or suggest a combination inclu ling "applying an electrical potential between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed." Applicants submit that *Yao* therefore cannot anticipate the claim and respectfully request withdrawal of the reje ion and allowance of the claim.

Ho discloses planarization by selective electro-dissolution. *Ho*, however, discl ses that only the metal layer should be removed by electro-dissolution. *Ho* instead discl ses that its barrier layer should be removed by etching or chemical-mechanical polis ing (CMP) (*see* paragraph [0039]). *Ho* therefore cannot disclose, teach or sugge t a combination including "applying an electrical potential between the wafer and an elect ode immersed in the electrolyte until at least part of the barrier layer is removed." Applic nts submit that *Ho* therefore cannot anticipate the claim and respectfully request withdraw l of the rejection and allowance of the claim.

Lopatin discloses a method of re-working copper damascene wafers. The layer 116 of *Lopatin* referred to by the Examiner is not a barrier layer at all, but is instead a diele tric layer (col. 5, lines 37-41). Layer 116 is also never removed. Layer 118 is referred t in *Lopatin* as a barrier layer, but this layer is applied directly to the dielectric (col. 5, lines 46-67); *Lopatin* therefore does not disclose a combination including "an inter-layer diele tric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier l yer deposited on the under-layer and a conductive layer deposited on the barrier lay er." Applicants submit that *Lopatin* therefore cannot anticipate the claim and respect lly request withdrawal of the rejection and allowance of the claim.

Claim 12, as amended, recites a process combination including:

> providing a wafer, *the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, and a barrier layer deposited on the under-layer, and a conductive layer deposited in the feature*;
>
> *placing the wafer in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer*;
>
> immersing the holder and the wafer in the electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte; and
>
> *applying an electrical potential between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed.*

(emphasis added). By analogy to the discussion above for claim 1, none of *Yao*, *H* · or *Lopatin*, disclose, teach or suggest every element and limitation of the claim. Applic .nts submit that *Yao*, *Ho* or *Lopatin* therefore cannot anticipate claim 12 and respectf ully request withdrawal of the rejection and allowance of the claim.

Claim 34, as amended, recites a process combination including:

> providing a wafer, *the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer*;

exposing the barrier layer; and

placing the wafer in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer;

immersing the holder and the wafer in the electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte; and

electrolytically removing at least part of the barrier layer using an electrolyte.

(emphasis added). By analogy to the discussion above for claim 1, none of *Yao*, *Ho* or *Lopatin*, disclose, teach or suggest every element and limitation of the claim. Applicants submit that *Yao*, *Ho* or *Lopatin* therefore cannot anticipate claim 34 and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 2-11, 13-22 and 35-44 if an independent claim is allowable, then any claim depending therefrom is also allowable. *See generally* MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, independent claims 1, 12 and 34 are in condition for allowance. Applicants submit that claims 2-11, 13-22 and 35-44 are therefore also allowable by virtue of their dependence on an allowable independent claims, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1-22 and 34-44 under 35 U.S.C § 103(a) as obvious in view of, and therefore unpatentable over, U.S. Patent No. 6,780,772 to Uzoh *et al.*

("*Uzoh*") in view of U.S. Patent Application Publication No. 2004/0072423 to Jorne *et al.* ("*Jorne*").

Applicants respectfully traverse the Examiner's rejections. To establish a *prima facie* case of obviousness, three criteria must be met: (1) the prior art references must teach or suggest all the claim limitations; (2) some suggestion or motivation to combine the references must be found in the prior art; and (3) there must be a reasonable expectation of success. MPEP § 2143. As explained below, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness.

Claim 1, as amended, recites a process combination including providing a wafer including a barrier layer, exposing the barrier layer, placing the wafer "in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer," placing the wafer in a base electrolyte such that at least the barrier layer is immersed in the electrolyte, and applying an electrical potential between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed. The Examiner concedes that *Uzoh* does not disclose the process details recited in the claims, but asserts that *Jorne* discloses the electropolishing details not disclosed in *Uzoh*, and that it would have been obvious at the time the present invention was made to combine *Uzoh* and *Jorne* to arrive at the present invention.

Applicants respectfully disagree. *Jorne* does not disclose the details of the claimed electropolishing process. *Jorne* teaches that the wafer W should be put in a wafer holder 54 (*see* Fig. 7b), but does not disclose, teach or suggest that wafer holder 54 seals the

edges of the wafer and insures that electrolytic solution only the surface of the w fer. *Jorne* therefore does not disclose, teach or suggest that the wafer should be placed ' n a holder that seals the edges thereof, such that, when the holder and the wafer are imme sed in an electrolyte, the electrolyte will only affect a surface of the wafer." *Uzoh* and *Jc ne*, taken together, therefore cannot disclose, teach or suggest a combination including the recited limitations. For the above reasons, Applicants submit that *Uzoh* and *Jorne* ca not obviate the claim. Applicants therefore respectfully request withdrawal of the reje ion and allowance of the claim.

Regarding claims 2-11, if an independent claim is non-obvious under 35 U.S. C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *I re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 1 is in condition for allowance. Applicants submit that claims 2-11 are therefore also allowable by virtu of their dependence on an allowable independent claim, as well as by virtue of the feat ures recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Claim 12, as amended, recites a process combination including providing a w fer comprising a barrier layer, placing the wafer "in a holder that seals the edges thereof, s uch that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will o nly affect a surface of the wafer." By analogy to the discussion above for claim 1, *Uzoh* and *Jorne*, when combined, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that *Uzoh* and *Jorne* therefore cannot obviate c im 12 and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 13-22, if an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 12 is in condition for allowance. Applicants submit that claims 13-22 are therefore also allowable by virtue of their dependence on an allowable independent claim, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Claim 34, as amended, recites a process combination including providing a wafer comprising a barrier layer, exposing the barrier layer, placing the wafer "in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer," and immersing the holder and the wafer in the electrolyte such that at least the barrier layer is wholly immersed in the electrolyte. By analogy to the discussion above for claim 1, *Uzoh* and *Jorne*, when combined, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that *Uzoh* and *Jorne* therefore cannot obviate claim 34, and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 35-44, if an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 34 is in condition for allowance. Applicants submit that claims 35-44 are therefore also allowable by virtue of their dependence on an allowable independent claim, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Conclusion

Given the above amendments and accompanying remarks, all claims pending in the application are in condition for allowance. If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to allowance of the claims the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

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Date: 7-5-06

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Enclosures: Amendment transmittal, in duplicate
Information Disclosure Statement and PTO-1449 form
One (1) cited IDS reference